Status of WP3: tasks

• **Task 3.1: Conceptual design of electronic front end**
  o Schedule M4-M6
  o Status: **completed**

• **Task 3.2: Design of the electronic front end system**
  o Schedule M7-M12
  o Status: **completed**

• **Task 3.3: Production of the electronic front end**
  o Schedule M13-M18
  o Status: **ongoing**

• **Task 3.4: Quality control and delivery of the electronic front end**
  o Schedule M19-M20
  o Status: **not started yet**
Status of WP3: deliverables

• **D 3.1: Front end system design**
  - Schedule M12
  - Status: *delivered*

• **D 3.2: Front End System prototype**
  - Schedule M20
  - Status: *not delivered*
Objectives of WP3

• **Hardware:**
  - New digitizer module: 12 or 14 bit @ 500 MS/s
  - Analog Bandwidth: ~250MHz
  - Software selectable input dynamic range (2 options: 0.5 and 2 Vpp)
  - Higher channel density (Desktop: 8 ch, VME: 16 ch)
  - Same readout interface of the old modules (VME, USB, Optical Link)

• **Firmware (DPP-PSD)**
  - Acquisition modes:
    - Oscilloscope mode (raw waveforms)
    - List mode (time stamp + integrated charges)
    - Mixed mode (list + oscilloscope)
  - On-line Coincidences
  - Pile-up detection/rejection
  - Event suppression based on PSD threshold
Status of the hardware development

• Schematics diagrams: 100% completed
• Bill of material completely defined
• PCB layout: almost terminated (final design review and check list): gerber files sent by 20\textsuperscript{th} of January.
• Next steps:
  o PCB manufacturing (\~10 prototypes)
  o Component procurement
  o Board assembly (2 prototypes)
  o Start of characterization tests (expected by end of March)
PCB layout: top layer (full board)
PCB layout: ADCs and FPGA (readout signals)
PCB layout: dual range analog input
Tests for the validation of the prototypes

- Power supply and heat dissipation
- Noise performances of the analog input stage
- Measurement of the Analog Bandwidth
- Dual range input
- Cyclone IV FPGA configuration (FW loading)
- Readout of ADCs (250 MHz DDR readout bus)
- Clock distribution, synchronization and jitter performance
- Max SRAM access frequency (required: 220 MHz!)
- Overall noise and distortion (ENOB)
- Linearity
- Temperature drift
- Test and measurements with a real setup
Acquisition System for MODES

- Three DT5730 (8x3 channels) directly connected to the detectors
- Independent channel triggering (self triggers)
- Coincidence between couple of channels
- No external trigger logic required
- On-line DPP for charge integration (Digital QDC)
- Dual gate (fast and slow component) for N-G discrimination (PSD)
- Waveform readout for photon counting (off-line)
- Mixed mode: save time stamp, charge and samples
- Synchronization between boards not required (to be confirmed)
Status of the firmware development

• 1st version of the FW (currently under development) for prototypes test (oscilloscope mode only, no DPP)

• Some problems to face:
  o Managing ADC synchronization (2 ns timing window)
  o Timing performance of the memory access: 220 MHz (previous boards didn’t exceed 180 MHz)
  o Sharing of trigger in-out lines between two channels
  o Data format (memory width = 140 bit = 10 samples, not a power of 2!)
  o ADC readout: DDR at 250MHz (same as x751 but with different timing)

• Final FW for Modes based on the DPP-PSD (Double Charge Integration) already developed for the x751 and x720 boards
DPP-PSD already developed for x751 and x720

- **Features:**
  - Three Acquisition Modes: oscilloscope, list, mixed
  - Independent Channel auto-trigger
  - Programmable waveform length and pre-trigger size
  - 32 bit trigger time stamp (1ns for x751, 4ns for x720)
  - Dual charge integration gate with programmable width and offset
  - PSD based on charge ratio (fast/slow component)
  - Dynamic Baseline Restorer
  - Pile-up detection and rejection
  - No dead time between triggers
DPP-PSD firmware: block diagram

\[ PSD = \frac{Q_{\text{LONG}} - Q_{\text{SHORT}}}{Q_{\text{LONG}}} \]
New features developed for MODES (on x751)

- **PSD cut:**
  - Keep only events whose PSD is over/under a programmable threshold.
  - Purpose: suppress gamma events => reduce data throughput
  - Data reduction needed when running in mixed mode (waveforms readout implies large event size)
  - Waveforms might be necessary in Modes for a better N/G discrimination based on photon counting instead of charge integration (do be tested with the new digitizer)

- **Coincidences:**
  - Each channel, when triggered on the input pulses, generates a trigger request signal of programmable width (= resolving time)
  - The main board combines the individual trigger requests (AND, OR or Majority) and generates individual trigger validations using different masks channel by channel
  - In Modes, coincidence between couple of channels will be used for the readout of two PMTs in a single tube in order to reduce false triggers (dark count, noise, etc...)
Coincidence Logic
Pile-up rejection: is it an issue?

- Single photon pulses in the signal tail generated by one gamma/neutron can be interpreted as a new pulse => real pile-up is difficult to detect
- The Gate integration is ~4us => how much is the probability of real pile-up?
- Is it necessary to manage pile-up in Modes?
- If so, pile-up rejection might be managed by the waveform post-processing
- Currently, the DPP-PSD firmware is able to detect (and reject) pile-up in the case where the trigger threshold is crossed again within the gate. It is necessary to prove that this technique is suitable for Modes
Synchronization between boards

- Cannels in the same DT5730 are already synchronized and the coincidence is managed at in the FPGA.
- Conversely, coincidences between channels from different DT5730 cannot be done at hardware level.
- Need post-processing with time stamp event correlation => boards must have same clock and start of run (= same $T_0$).
- Latest firmware versions of the DPP-PSD support synchronization through Trigger IN-OUT daisy chain.
- Unlike VME, Desktop version doesn't feature Clock IN-OUT daisy chain => it would be necessary to implement an external clock generator and fan-out.
Tests at Arktis (December 2012)

• **Test Setup:**
  - One $^4$He tube with 2 PMTs connected to the digitizer
  - One 4 slot VME crate
  - One V1751 (8 channel, 10 bit, 1GS/s digitizer)
  - One V1718 (USB to VME bridge) connected to a Linux PC through the USB port
  - One V6533 (6 channel, 3kV, High Voltage Power Supply) biasing the PMTs
  - DPP-PSD Firmware with new features
  - DAQ developed by INFN PD

• **Purpose:**
  - Test the coincidence between two channels
  - Measure overall throughput rate
  - Test N/G separation (Figure Of Merit of the PSD)
  - Test PSD cut with different thresholds
  - Compare results previously obtained with an 8 bit, 500MS/s digitizer (V1731)
  - Compare on-line analysis (charge integration only) with off-line post processing of the waveforms (photon counting)
  - Test and tuning of the DAQ
  - It was no possible to test Pile-Up rejection because of the low counting rate
Next Steps

• **Hardware:**
  - PCB manufacturing: February
  - Component procuring and prototype assembly (2 pcs): March
  - Test and characterization: April
  - Rework and Validation: May
  - Production: June

• **Firmware:**
  - Feedback from tests with Modes detectors: February
  - Basic firmware development (oscilloscope mode) for DT5730: April
  - DPP-PSD proto version: June
  - Final DPP-PSD firmware development: August
The WP3 Activities in MODES_SNMM

Task 3.1 - Conceptual design of the electronic front-end - **COMPLETED**
- Leader: CAEN; Contributors: ARKTIS, UINS
- Task schedule: M4-M6
- CAEN, together with ARKTIS and UINS, will choose the more suited technology (type of digitizer, type of digital filtering) to perform the read out of the SiPM detector matrix and for PMTs.

Task 3.2 - Design of the electronic front-end system including DAQ – **RECENTLY COMPLETED**
- Leader: CAEN; Contributors: UINS
- Task schedule: M7-M12
- Design will involve mainly the firmware in the digitizer module that will be chosen, but likely even some characterization of the hardware implementation. UINS and CAEN have a previous agreement to develop read out applications based on SiPM, so the design will be carried out together. This design will flow in a technical report (D3.1).

Task 3.3 - Production of the electronic front-end - **STARTED**
- Leader: CAEN; Contributors: -
- Task schedule: M13-M18
- This task will include the realization of the PCB and the complete mounting of all the equipments needed to carry out the data acquisition from the detector.

Task 3.4 - Quality control and delivery of the electronic front-end
- Leader: CAEN; Contributors: UINS
- Task schedule: M19-M20
- All the devices will be tested by CAEN and UINS so to be qualified before being shipped to the integration facilities.

**Deliverables**
- D3.1 Front-end System Design (M12) – Report – **COMPLETED**
- D3.2 Front-end System Prototype (M20) - Prototype

**Milestones**
- MS8 Read-out Electronics (Performances accomplishment) – M20